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| EXAMINER |
|---|
| HERNANDEZ, WILLIAM |

| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/796,859 | STIFF ET AL. | |
| | Examiner | Art Unit | |
| | William Hernandez | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5-9,11 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5 and 21* is/are allowed.

6)☒ Claim(s) *6-9,11,13-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's amendment has been received and entered in the case. The amendments and arguments presented therein overcome the informality objections, and therefore, these are withdrawn. However, the amendments and arguments do not overcome all the prior art rejections nor the indefiniteness rejections, and therefore, these are maintained.

### *Drawings*

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the pull-down transistor being coupled to the floating current mirror must be shown in Fig. 2 or the feature canceled from claim 11. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. Claim 6 is objected to because of the following informalities:

In the last line of claim 6, the phrase "a ground node" should read --supply voltage node--. The source node of each transistor not being directly to the ground node was already mentioned in the previous two lines.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11, 13, 15-20 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 11, the limitation, "wherein the pull-down transistor has one end coupled with the floating current mirror" is misdescriptive. This is not shown in Fig. 2 of Applicant's drawings. One end of the pull-down transistor (M3) is shown coupled to

ground (vgnd) while the other end is shown coupled to the gate of another transistor (M6) which in turn is coupled to the floating current mirror (M4 and M5). Since the pull-down transistor is coupled to the gate of an intervening transistor, there can be no conductive path to the floating current mirror; thus, the pull-down transistor is **not coupled** to the floating current mirror.

Claims 13, 15-20 and 22 are rejected for inheriting the indefiniteness of parent claim 11.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwak et al. (USP 7,064,601 B2).

As to claim 6, Kwak's Fig. 3 shows a method for providing a current reference, comprising:

providing a current mirror circuit portion (140) having a plurality of transistors, wherein each source node of said plurality of transistors forming the current mirror are

directly coupled together (clearly shown), wherein the source node of each transistor forming the floating current mirror is not directly coupled to a ground node (clearly shown), and wherein the source node of each transistor forming the floating current mirror is not directly coupled to a ground node (clearly shown);

providing a positive feedback loop portion (160) coupled with the current mirror circuit portion;

providing a negative feedback loop portion (120) diverting current from the current mirror circuit portion; and

operating the current reference with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages (a floating current mirror does not require the additional MOSFET threshold used by a typical current mirror).

As to claims 7, 8 and 9, the recited limitations are clearly shown in Kwak's Fig. 3.

8. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Kobatake (USP 6,204,724 B1).

Kobatake's Fig. 8 shows a circuit providing a current reference, comprising:

a floating current mirror (the emitters are not coupled to ground directly) including a first transistor (P2) and a second transistor (P1);

at least one resistor (R1) defining a voltage node;

a pull-down transistor (N25); and

an output transistor (P3);

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor P2 is coupled to resistor R1 via transistor N2);

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor P1's gate is coupled to the gate of output transistor P3);

wherein a source node of the first transistor is directly coupled to the source node of the second transistor (clearly shown);

wherein the source nodes of the first and second transistors are not directly coupled to a ground node or a supply voltage node (the source nodes are coupled to Vdd1 which is not a supply voltage node but an intermediate voltage located between the source nodes and the actual supply voltage Vdd);

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor ($I_2$ and $I_1$ are mirrored currents); and

wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages (a floating current mirror does not require the additional MOSFET threshold used by a typical current mirror) as called for in claim 14.

***Response to Arguments***

9. Applicant's arguments filed 8/16/07 have been fully considered but they are not persuasive.

Regarding claim 6, Applicant argues that Kwak fails to teach or suggest either the coupling together of the source nodes of the transistors forming the current mirror and the source nodes not directly coupled to a ground node or a supply voltage node. However, the claim as currently amended, does not recite the source nodes not directly coupled to a supply voltage node. Therefore, the Kwak reference continues to read on claim 6.

Regarding claim 11, Applicant argues that the floating current mirror is "coupled" with the pull-down transistor based on the ordinary meaning of the word "coupled"; however, this is not shown in Applicant's Fig. 2. The ordinary meaning of the word "coupled" would require that there be a conductive path between the pull-down transistor (M3) and the floating current mirror (M4 and M5), yet there is a gate connection (to transistor M6) between the pull-down and the floating current mirror blocking any current between the two.

Regarding claim 14, Applicant argues that Kobatake fails to teach or suggest either the coupling together of the source nodes of the transistors forming the current mirror and the source nodes not directly coupled to a ground node or a supply voltage node; Examiner respectfully disagrees with this assertion. Clearly shown in Kobatake's Fig. 8, the source nodes of transistors P1 and P2 are coupled together and they are also not directly coupled to either the ground node or the supply voltage node (Vdd).

In summary, the amendments to the claims were not limiting enough to overcome the Kobatake reference and the 112 2nd rejection of claim 11 has not been addressed satisfactorily in view of Applicant's Fig. 2.

***Allowable Subject Matter***

10. Claims 11, 13, 15-20 and 22 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest the limitation of "wherein each source node of the plurality of transistors forming the floating current mirror are directly coupled together; wherein the source node of each transistor forming the floating current mirror is not directly coupled to a ground node; and wherein the source node of each transistor forming the floating current mirror is not directly coupled to a supply voltage node" as called for in independent claim 1. Therefore, claims 1-5 and 21 are presently allowed.

***Conclusion***

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WH

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER